

Lesson Planning for the semester started w.e.f. 5th Jan. 2018.

Name of Institute :- Sat Kabir Institute of Technology and Management, Ladrawan (Jhajjar)

Name of teacher with designation :- SUMIT DALAL, A.P.

Department :- ECE

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
JAN	ECE-4 th Sem	<u>Comm. Systems</u> : Introduction to Communication systems (1-2 week) Basic concept of Modulation, Demodulation, MUX & DEMUX. (3-4 weeks)	Ppt. Section revision	Assignment in 3 rd week Test in 4 th week
JAN.	ECE-6 th Sem	<u>VLSI Design</u> : Basic MOS transistor - E-mode & De-mode. (2 weeks) Second order effect - MOS transistor Model. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
JAN	MTech 2 nd Sem	<u>VLSI design</u> : Review of MOS technology. (2 week) N-MOS, CMOS process, Production of masks. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
FEB	ECE-4 th Sem	<u>Comm Systems</u> : Amplitude Modulation - Generation, demodulation, USB (2 week) Angle Modulation - PM, FM, NBFM, WBFM. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
FEB	ECE-6 th Sem	<u>VLSI Design</u> : N-MOS & CMOS Inverter & gates. (2 weeks) Stick diagram - Lambda based design rules (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
FEB	MTech 2 nd Sem	<u>VLSI Design</u> : Electrical Properties of MOS circuit (2 week) MOS Transistors Model, Pull-up to pull-down ratio. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
MARCH	ECE-5 th Sem	<u>Comm Systems</u> : Pulse Analog modulation, Multiplexing Techniques (2 week) Pulse Digital modulation, DPCM, DM. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
	ECE-6 th Sem	<u>VLSI Design</u> : Sub-system design & layout (2 week) NAND-NAND, NOR-NOR, AOI logic - (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week
	MTech 2 nd Sem	<u>VLSI Design</u> : Design processes, Mos layer, Stick diagram (2 week) Basic circuit-carabits - Sheet resistance, type of delays. (2 week)	Ppt Section revision	Assignment in 3 rd week Test in 4 th week


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Department :- E.C.E.

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
APRIL	ECE-4 th Sem	Comm System: Digital Modulation Techniques - ASK, FSK, BPSK, QPSK. (2week)	Ppt	Assignment in 3 rd week
		Introduction to Noise - External, internal noise, S/N ratio. (2week)	Section revision	Test in 4 th week
ECE-5 th Sem	VLSI Design:	Design of combinational elements & Regular array logic. (2week)	Ppt	Assignment in 3 rd week
		VHDL programming - operators, packages, FSM, Demux (2week)	Section revision	Test in 4 th week
ECE-2 nd Sem	VLSI Design:	Subsystem, Design and layout (2week)	Ppt	Assignment in 3 rd week
		Design examples - design of ALU subsystems. (2week)	Section revision	Test in 4 th week

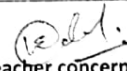

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Name of Institute :- Sat Kabir Institute of Technology and Management, Ladrawan (Jhajjar)

Name of teacher with designation :- SOMIT DALAL, AP.

Department :- ECE

Month	Class	Topic/Chapter Covered	Academic Activity	Test/Assignment
JAN.	ECE 4 th	CS LAB :-> 1. Generation of DSB-SC AM signal using Balanced modulators. 2. Generation of SSB-AM signal 3. To study envelope detectors for demodulation of AM signal.	Practical to be performed	File to be checked
JAN	M Tech 2 nd Sem	VLSI lab :-> 1. Write a spice programme for CMOS inverter. 2. Write a spice programme for CMOS NAND gate 3. Write a spice programme for CMOS NOR gate.	Practicals to be performed	File to be checked.
FEB	ECE 4 th	CS LAB :-> 1. Freq. Modulation using VCO. 2. Detection of FM using PLL & Foster-Seeley method. 3. To study ckt of PAM/PWM/PPM mod & demodulators.	Practicals to be performed	File to be checked.
FEB	M Tech 2 nd Sem	VLSI lab :-> 1. Design a D-latch with clk time-period. 2. Design a half-adder using NAND gates 3. Design layout for PMOS in layout editor	Practicals to be performed	File to be checked.
MAR	ECE 4 th Sem	CS LAB :-> 1. Generation & study of Analog TDM four channels 2. Study of ASK, FSK mod. & demodulators. 2. Study of PSK & QPSK Mod. & demodulators.	Practicals to be performed	File to be checked.
MAR	M Tech 2 nd Sem	VLSI lab :-> 1. Design layout for NMOS in layout editor 2. Design layout for CMOS inverter. 3. Design layout for 2-input NAND gate.	Practicals to be performed	File to be checked.
APR.	ECE 4 th Sem	CS LAB :-> 1. Study of PCM mod & demodulation 2. Practical problems & viva.	Practical to be performed	File to be checked.
APR.	M Tech 2 nd Sem	VLSI lab :-> 1. Design layout for 2-input NOR gate 2. Practical problems & viva.	Practical & Viva performed	File to be checked.


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